DATA SHEET

SVPL3R312SG SERIES

SPACE QUALIFIED POINT OF LOAD CONVERTERS



SVPL Series DC-DC Converter

Models Available
Input: 3.1 V to 5.5 V
12 A output
Qualified to MIL-PRF-38534 Class H and Class K

1.0 DESCRIPTION

The SVPL Series of space qualified point-of-load DC-DC converters is specifically designed for the harsh radiation environment of space applications. Performance is guaranteed through the use of hardened semiconductor components and analysis. The SVPL Series has been characterized for Total Ionizing Dose (TID) performance including Enhanced Low Dose Rate Sensitivity (ELDRS) and for Single Event Effects (SEE) per VPT's DLA-approved Radiation Hardness Assurance (RHA) plan per MIL-PRF-38534, Appendix G, Level R.

The SVPL3R312SG is based on the Intersil ISL70002SEH radiation-hardened monolithic buck regulator. It is designed to operate from a nominal 3.3 V or 5 V bus. The SVPL3R312SG supplies low voltages at 12 A with high efficiency and fast transient response, making it an ideal choice to supply point-of-load applications such as high performance space processors.

1.1 FEATURES

- Operates from 3.1 – 5.5 V input
- Adjustable Output from 0.8 – 3.8 V
- Up to 12 Amps Output
- High Efficiency, up to 93%
- High Power Density, up to 134 W/in^3
- Output Enable Control
- Low Output Noise
- Over Current Protection
- Bi-directional SYNC pin allows devices to be synchronized 180° out-of-phase

1.2 SPACE LEVEL CHARACTERIZATIONS

- Total Ionizing Dose Performance
  - High Dose Rate [50-300 rad(Si)/s] ≥ 100 krad(Si)
  - Low Dose Rate [<10 mrad(Si)/s] ≥ 100 krad(Si)
- Single Event Effects Performance
  - SEL, SEB, and SEGR LET_{TH} ≥ 85 MeV-cm^2/mg
  - SEFI Threshold LET_{TH} ≥ 58 MeV-cm^2/mg
  - SEFI X-section (LET_{EFF} = 85 MeV-cm^2/mg) ≤ 6.59x10^{-7} cm^2
  - SET fully characterized for cross section and magnitude
- Operation from -55 °C to +125 °C
- Worst-case analysis, stress, radiation, reliability reports available

1.3 MANUFACTURING AND COMPLIANCE

- Qualified to MIL-PRF-38534 Class H and Class K, DLA SMD # 5962-17217
- MIL-PRF-38534 element evaluated components
- Manufactured in a MIL-PRF-38534 Class H and Class K facility
- MIL-STD-883
- ISO-9001

1.4 PACKAGING

- Low-profile: 1.110" x 1.110" x 0.276"
- Max weight: 22 g
- Precision seam-welded hermetic metal case
- Standard gullwing or optional straight-lead versions available

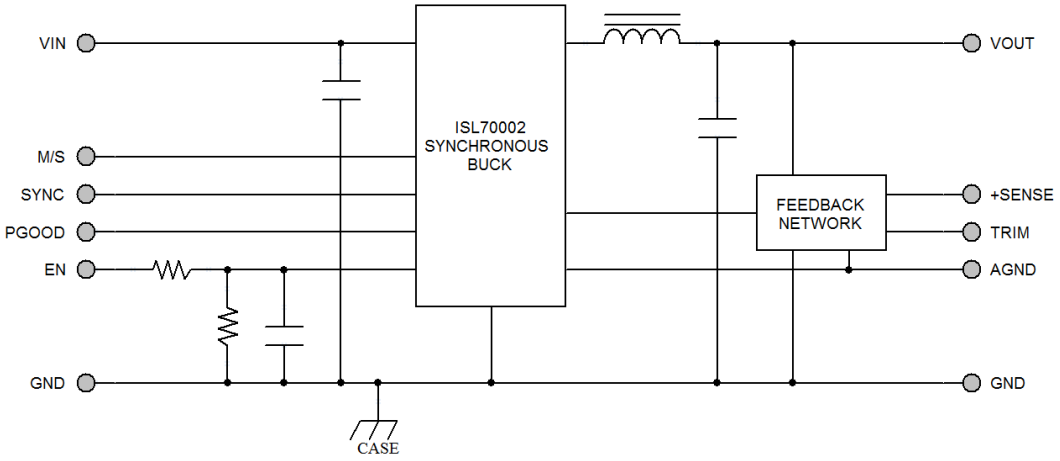
1.5 SIMILAR PRODUCTS AND ACCESSORIES

- SVGA0515S 15 A space qualified point of load DC-DC converter
- SVRGA0508S 8 A space qualified point of load DC-DC converter
- Custom versions available
- Space qualified isolated DC-DC converters, 6 - 100 W
- EMI filters

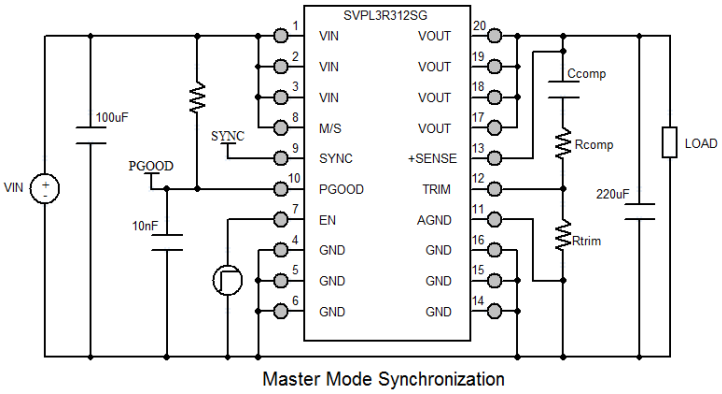
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2.0 DIAGRAMS

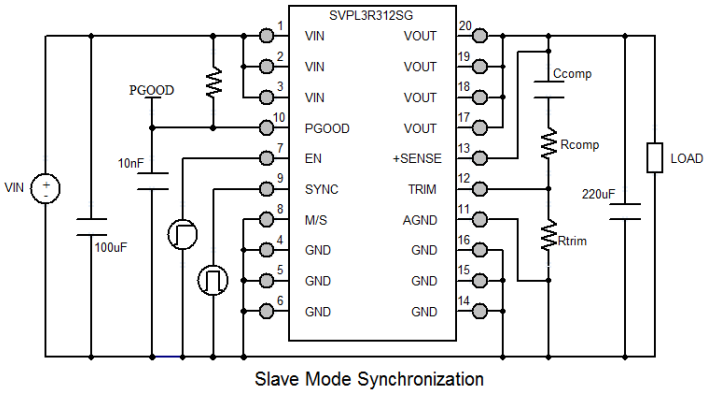
2.1 BLOCK DIAGRAM



2.2 CONNECTION DIAGRAMS



Master Mode Synchronization



Slave Mode Synchronization

1. Rtrim should be connected directly across pins 11 and 12 as close as possible to the SVPL.
2. AGND should be connected to GND close to the SVPL. Voltage difference between the AGND and the GND pins greater than 0.3 V may result in regulation error and/or damage to the SVPL.
3. If not using EN, connect pin 7 to VIN.
4. If not synchronizing converters, use Master Mode Synchronization connections and leave pin 9 open.
5. If not using PGOOD, leave pin 10 open.
6. Rcomp and Ccomp are optional components that can be used to optimize the SVPL transient response.

3.0 SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings			
VIN, PGOOD[1]:	-0.3 V to 6.5 V	Operating Temperature (Full Load):	-55 °C to +125 °C
EN, M/S, SYNC	-0.3 V to Vin + 0.3 V	Storage Temperature:	-65 °C to +150 °C
AGND	-0.3 V to 0.3 V	Lead Solder Temperature (10 seconds):	270 °C
ESD Rating per MIL-PRF-38534:	1 A	Solder Reflow Temperature (30 seconds):	220 °C

1. Limited to 6.2 V for operation in a heavy ion environment at LET ≥ 85 MeV-cm^2/mg and Tcase = 125 °C.

3.2 PERFORMANCE SPECIFICATIONS[1]

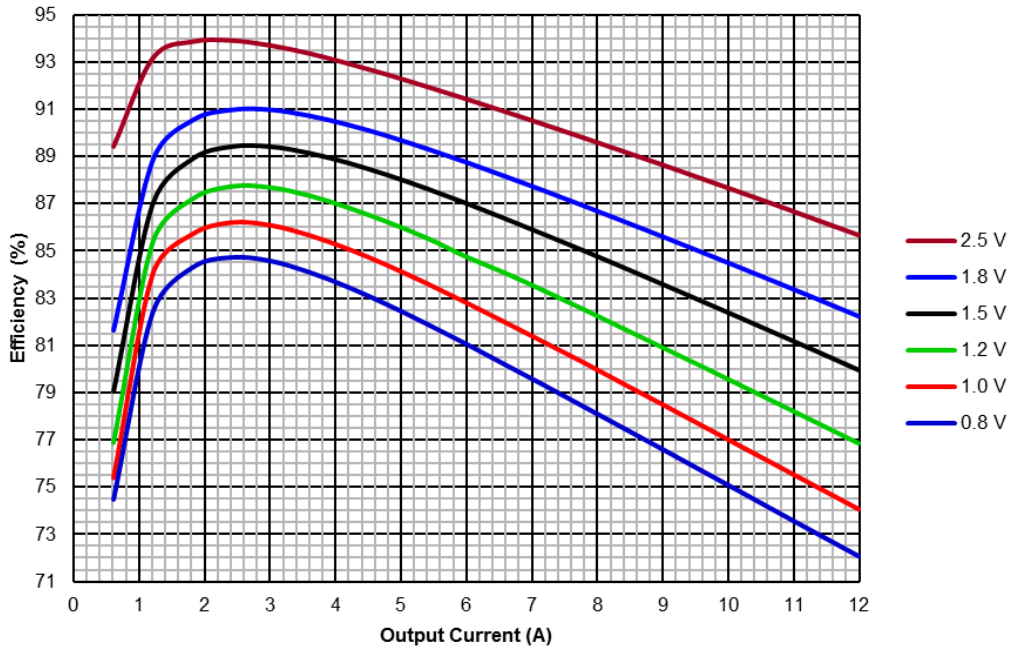
Tcase = -55 °C to +125 °C, Vin = +5 V ± 1% or 3.3 V ± 1%, Full Load, Unless Otherwise Specified

		SVPL3R312SG			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Units**
INPUT					
Voltage[2]		3.1	-	5.5	V
Current	EN = GND, Vin = 5 V	-	5.5	10	mA
	EN = GND, Vin = 3.3 V	-	4.5	10	mA
	EN = Vin = 5 V, No Load	-	85	130	mA
	EN = Vin = 3.3 V, No Load	-	50	70	mA
Undervoltage Lockout	Rising Threshold[2]	2.65	2.8	2.95	V
	Hysteresis[2]	0.07	0.14	0.24	V
OUTPUT STATIC					
Voltage	Tcase = 25 °C	-1.0	-	+1.0	%Vout
	Tcase = -55 °C to +125 °C	-1.5	-	+1.5	%Vout
Power[3]		0	-	45.6	W
Current		0	-	12	A
Ripple Voltage	20 Hz to 10 MHz	-	25	50	mVpp
Load Regulation		-0.5	0.03	+0.5	%Vout
Load Fault Dissipation	Vin = 5 V, Vout = 3.3 V	-	-	2	W
OUTPUT DYNAMIC					
Load Step, Half to Full Load, Vout = 3.3 V	Output Transient	-	75	140	mV
	Recovery[4]	-	150	300	µs
Turn-On (Vin = 0 to 3.3 V or 5 V, EN = Vin)	Delay	-	6.5	12	ms
	Overshoot	-	0	15	mVpk
FUNCTION					
Enable (EN)[2]	Rising Threshold	1.15	1.31	1.48	V
	Hysteresis	0.058	0.110	0.172	V
	EN Pin Current, EN = 5.5 V	-	-	300	µA
SYNC Frequency Range	Vin = 5 V, M/S = GND	425	500	575	kHz
GENERAL					
Efficiency	Vin = 5 V, Vout = 3.3 V, Iout = 12 A	83	88	-	%
Capacitive Load[2]	Vout ≤ 2 V	220	-	5000	µF
	Vout ≥ 2V	220	-	$\frac{10000}{Vout}$	µF
Switching Frequency	M/S = Vin	425	500	575	kHz
Weight	Standard package option	-	-	22	g
MTBF (MIL-HDBK-217F)	SF @ Tcase = 55 °C	-	7.13	-	MHr
POST-RAD END-OF-LIFE LIMITS[5]					
OUTPUT Voltage	Tcase = -55 °C to +125 °C	-3.0	-	+3.0	%Vout

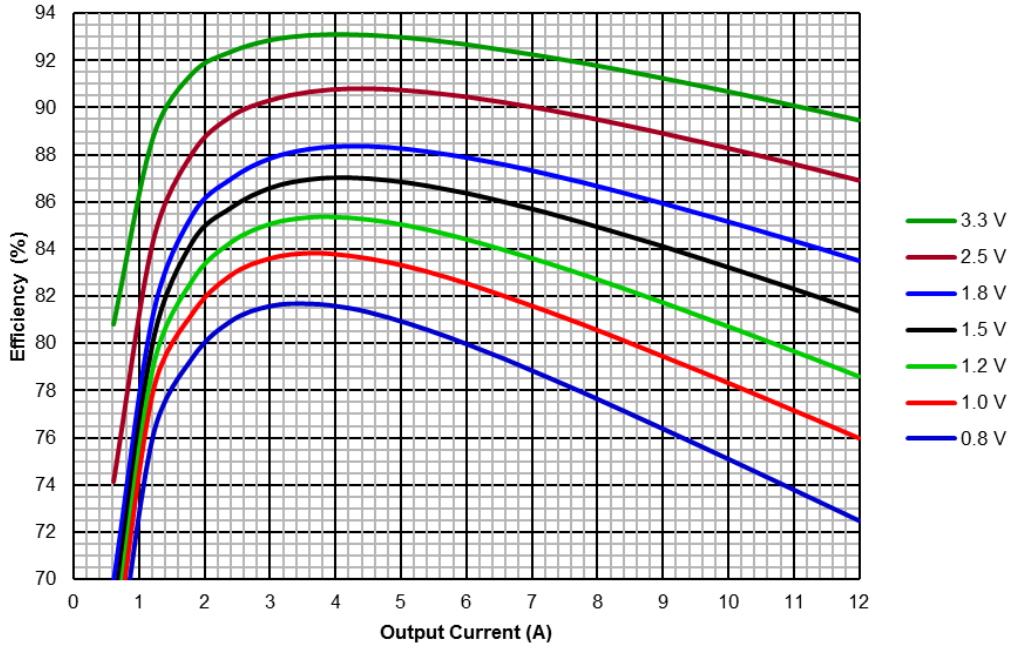
1. Performance specifications are guaranteed with 100 µF from VIN to GND and 220 µF from VOUT to GND
2. Verified by qualification testing
3. Dependent on output voltage
4. Time for output voltage to settle within 1% of steady-state value
5. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted

4.0 PERFORMANCE CURVES

4.1.1 SVPL3R312SG Efficiency (Typical, 25 °C, Vin = 3.3 V)

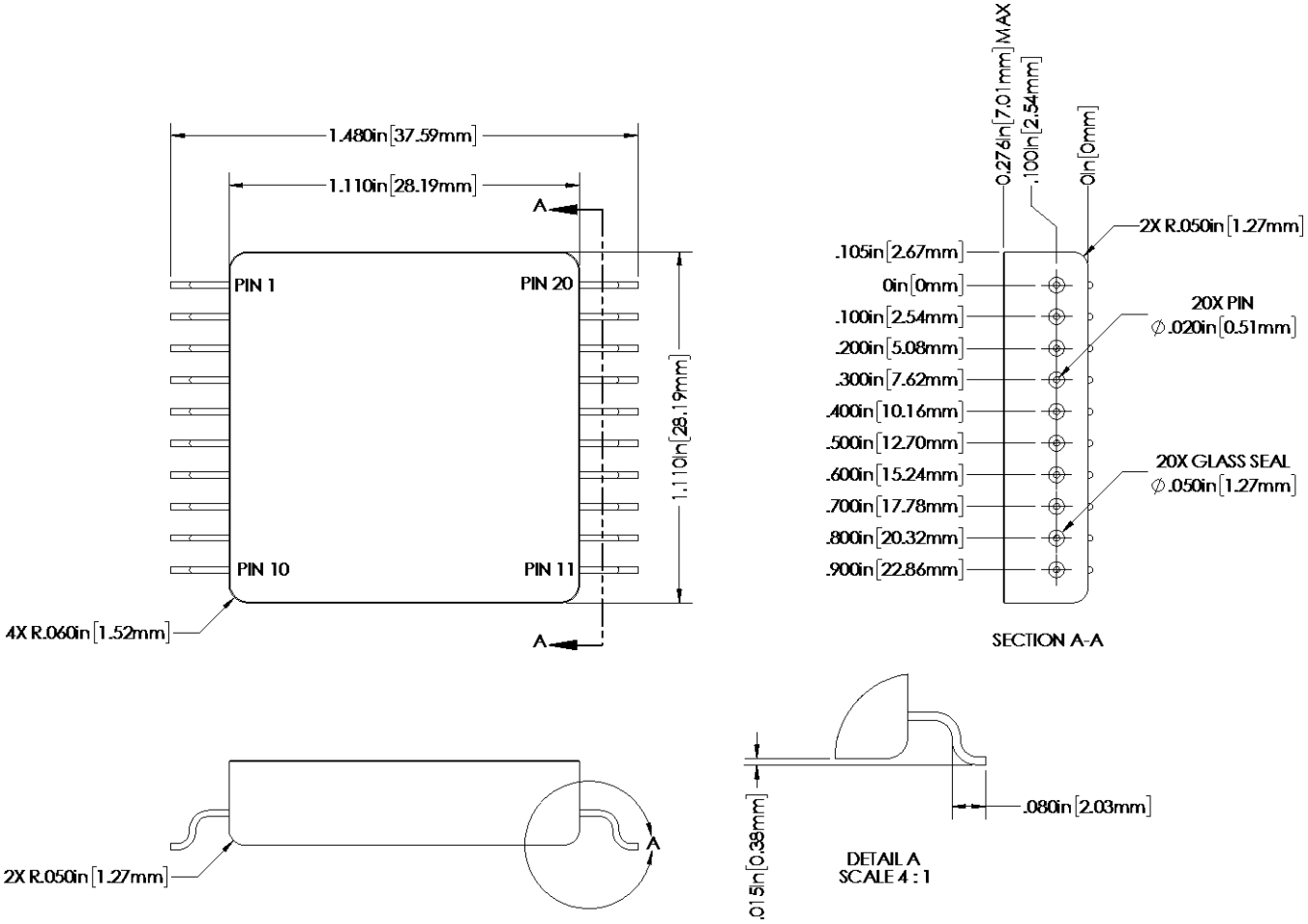


4.1.2 SVPL3R312SG Efficiency (Typical, 25 °C, Vin = 5 V)



5.0 MECHANICAL OUTLINES AND PINOUT

Standard Gullwing Package Option:

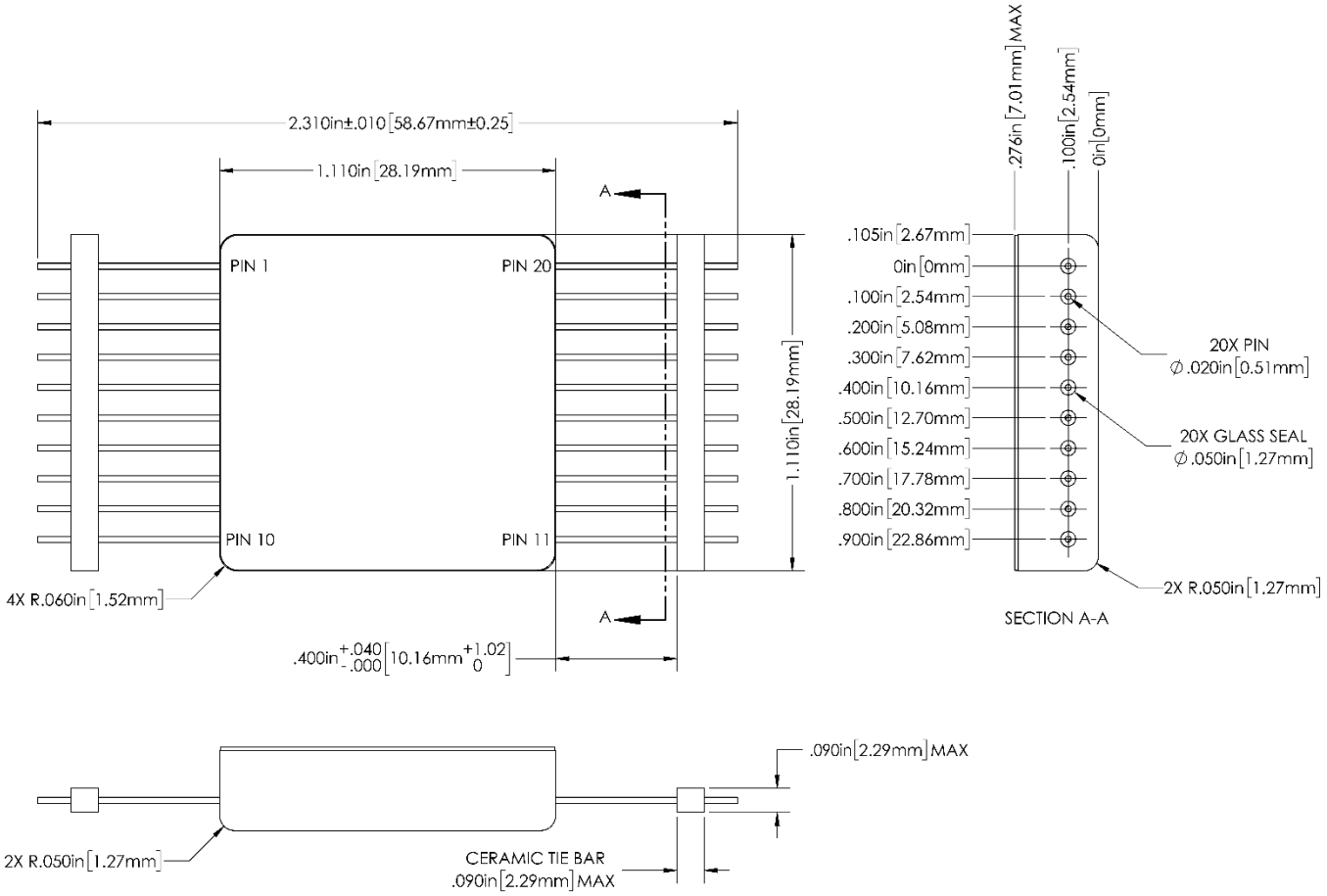


1. Tolerances are +0.005" unless otherwise stated
2. Case temperature is measured on the center of the baseplate surface
3. Materials: Case (Steel, gold over nickel plated); Cover (Steel, nickel plated); Pin (Copper-cored alloy 52, gold over nickel plated, 63/37 SnPb solder dipped); Pin Seals (Glass)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	VIN	6	GND	11	AGND	16	GND
2	VIN	7	EN	12	TRIM	17	VOUT
3	VIN	8	M/S	13	+SENSE	18	VOUT
4	GND	9	SYNC	14	GND	19	VOUT
5	GND	10	PGOOD	15	GND	20	VOUT

5.0 MECHANICAL OUTLINES AND PINOUT (CONTINUED)

Optional Straight-Lead Package:



1. Tolerances are +0.005" unless otherwise stated
2. Case temperature is measured on the center of the baseplate surface
3. Materials: Case (Steel, gold over nickel plated); Cover (Steel, nickel plated); Pin (Copper-cored alloy 52, gold over nickel plated); Pin Seals (Glass)
4. Pins may have exposed nickel plating (not base metal) beyond the ceramic tie bars due to the plating process. No nickel plating is exposed between the tie bar and case.

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	VIN	6	GND	11	AGND	16	GND
2	VIN	7	EN	12	TRIM	17	VOUT
3	VIN	8	M/S	13	+SENSE	18	VOUT
4	GND	9	SYNC	14	GND	19	VOUT
5	GND	10	PGOOD	15	GND	20	VOUT

6.0 TECHNICAL NOTES



Please note that many of these functions are also demonstrated in detail on the VPT website in the form of technical video labs.

6.1 GENERAL INFORMATION

6.1.1 Topology Description

The SVPL3R312SG is a non-isolated, fixed-frequency, radiation-hardened, synchronous buck converter based on the Intersil ISL70002SEH. It is optimized for low voltage point-of-load (POL) applications. The SVPL3R312SG operates from a 3.1 to 5.5 V input and provides a stepped-down, precisely regulated, programmable output voltage at high efficiency.

6.1.2 Source Impedance

The impedance of the 3.3 V or 5 V source can interact with the POL converter and impact performance. High source impedance is often caused by a long input cable or other components added in series with the input. In some cases, additional input capacitance will be needed to stabilize the system.

6.1.3 Case Connection

The SVPL3R312SG case is connected to GND at a single point inside of the package.

6.2 FUNCTION DESCRIPTIONS

6.2.1 Enable (EN)

The figure below demonstrates the enable circuit. Initially, $V_{control}$ is below the turn-on threshold ($V_{control_enable}$), and the I_{en} current source is active. As $V_{control}$ rises, the turn-on threshold is calculated as:

$$V_{control_enable} = V_r \cdot \left[1 + \frac{R_1 + R_{en}}{R_2}\right] + I_{en} \cdot (R_1 + R_{en})$$

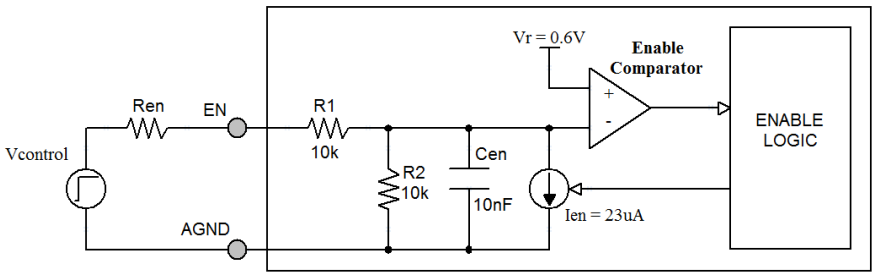
After $V_{control}$ reaches $V_{control_enable}$, I_{en} turns off. To disable the converter, drive $V_{control}$ below the turn-off threshold ($V_{control_disable}$):

$$V_{control_disable} = V_r \cdot \left[1 + \frac{R_1 + R_{en}}{R_2}\right]$$

The enable circuit hysteresis is:

$$V_{control_hys} = V_{control_enable} - V_{control_disable} = I_{en} \cdot (R_1 + R_{en})$$

When EN is driven directly from a low-resistance source, R_{en} can be assumed to be 0 Ω, and the limits from the Performance Specifications table apply directly. To increase the turn-on threshold, add the appropriate R_{en} based on the equations above. If the ability to disable the SVPL3R312SG is not necessary, connect EN to VIN. When EN is below its turn-on threshold, the internal power MOSFETs are turned off, and the SVPL3R312SG power stage is in a high-impedance state.



6.2.2 Power Good (PGOOD)

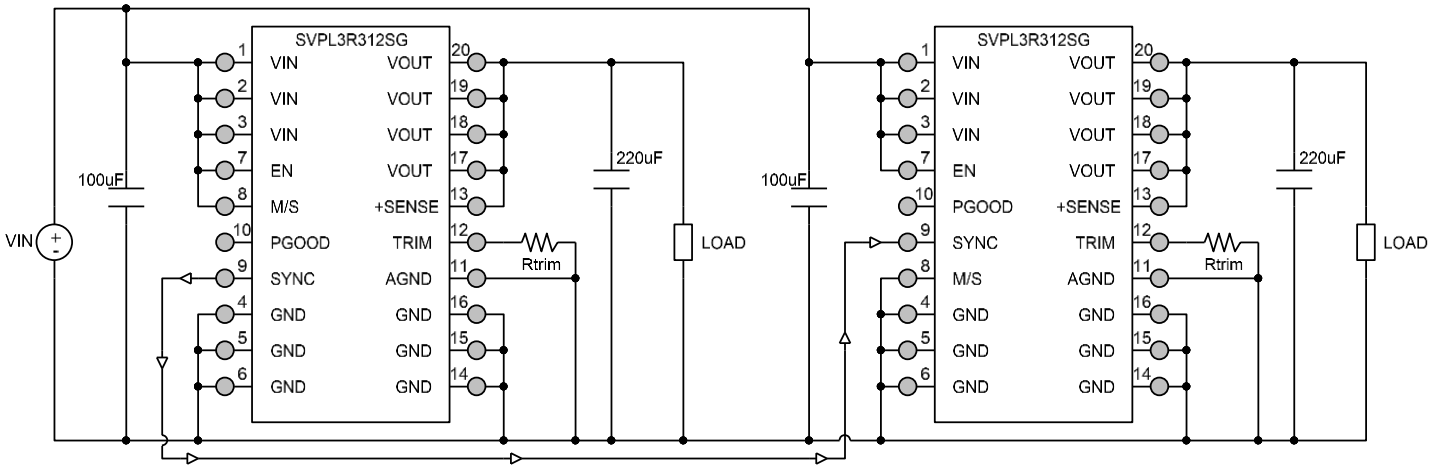
PGOOD is an open-drain output. It is pulled to GND when the output voltage is outside a ±11% regulation window. When the output voltage is within ±11% of its set point, PGOOD will be released. The PGOOD pin can be pulled up through an external resistor to any voltage from 0 to 5.5 V, independent of the input voltage. The external pull-up resistor should have a nominal value in the range of 1 kΩ to 10 kΩ.

6.2.3 Synchronization (M/S and SYNC)

When multiple DC/DC converters are connected to a common input bus, differences in their switching frequencies may lead to undesired beat frequencies at the common bus. The simplest way to mitigate beat frequency issues is to synchronize the POL converters.

To synchronize two or more SVPL3R312SG converters:

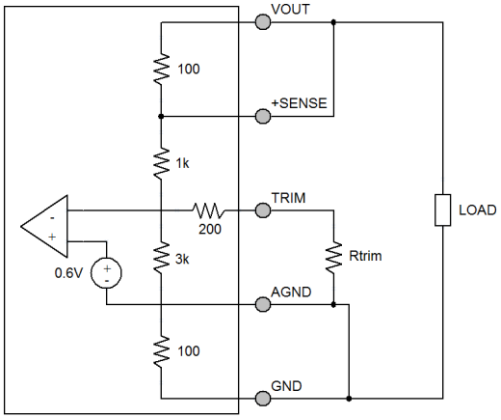
- Connect the M/S pin of the master converter to VIN (SYNC will output pulses with magnitude of VIN and 50% duty cycle)
- Connect the M/S pin of the slave converters to GND (SYNC will be configured as an input)
- Connect the SYNC pins of the master and slave converters together



To synchronize to an external clock, connect M/S to GND and connect the clock output to SYNC. The clock signal's low level must be less than 1 V and its high level must be between 2.3 V and VIN to guarantee proper synchronization. Its duty cycle should be between 40 to 60%. If not synchronizing converters, connect M/S to VIN and leave SYNC open.

6.2.4 Adjusting the Output Voltage (TRIM)

The output voltage of the converter is set with an external trim resistor connected from the TRIM pin to the AGND pin. Use the equations or table below to choose the trim resistor value. Trim resistor tolerance of 0.1% is recommended to achieve an accurate output voltage. The default output voltage with the TRIM pin left open is 0.8 V. The designer can adjust the output voltage from 0.8 V to 85% of the input voltage.



$$R_{trim} = \frac{600}{V_{OUT} - 0.8} - 200$$

$$V_{OUT} = \frac{600}{R_{TRIM} + 200} + 0.8$$

SVPL3R312SG	
+Vout (V)	**Rtrim (Ω)**
0.8	Open
0.9	5.80k
1.0	2.80k
1.2	1.30k
1.5	657
1.8	400
2.0	300
2.5	153
2.8	100
3.0	72.7
3.3	40.0
3.6	14.3
3.8	0.0

6.2.5 Output Capacitors

While the SVPL3R312SG is stable without external output capacitance, a minimum of 220 µF is required to meet the Performance Specifications from section 3.2. Output capacitors for point-of-load (POL) DC/DC converters should be chosen to meet output voltage ripple and transient requirements. Meeting the transient response requirement is accomplished by making the output impedance of the converter sufficiently small. Given the high control bandwidth of POL converters like the SVPL series, the peak output impedance is typically dominated by the equivalent series resistance (ESR) of the bulk output capacitance. Therefore, the output capacitors should be chosen to set a certain maximum total ESR. The total ESR is the parallel combination of the internal bulk capacitor's ESR and that of the added capacitors. Given the output voltage transient requirement, maximum load step, and the ESR of each bulk capacitor that will be added, the number of added capacitors needed is calculated with the following equations:

$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}}$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}}$$

Parameter	Definition
ΔV_{OUT}	Max V_{OUT} transient allowed
ΔI_{OUT}	Max load current step
ESR_{TOTAL}	Total combined parallel ESR, including internal and added capacitors
ESR_{ADDED}	Combined parallel ESR of the added capacitors
$ESR_{INTERNAL}$	ESR of the internal bulk capacitor (**43.7mΩ max** under worst-case conditions)
ESR_{EACH}	ESR of each of the added capacitors
N	Number of added capacitors

For example, assume that V_{OUT} is 1.5 V, the maximum output transient allowed is 37.5 mV, and the load step is 6 A. Assume the output capacitors being used are 330 µF and have a maximum ESR of 50mΩ each.

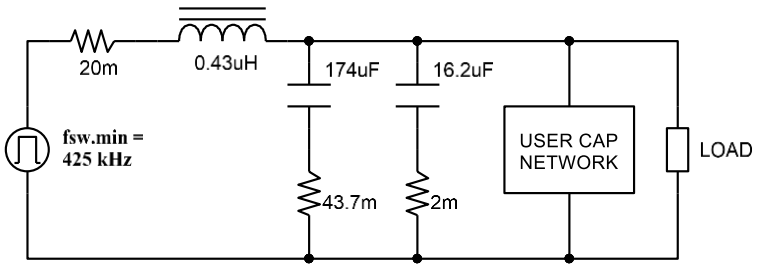
$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{37.5mV}{6A} = 6.25m\Omega$$

$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}} = \frac{6.25m\Omega * 43.7m\Omega}{43.7m\Omega - 6.25m\Omega} = 7.29m\Omega$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}} = \frac{50m\Omega}{7.29m\Omega} = 6.86 \rightarrow use\ 7\ output\ capacitors$$

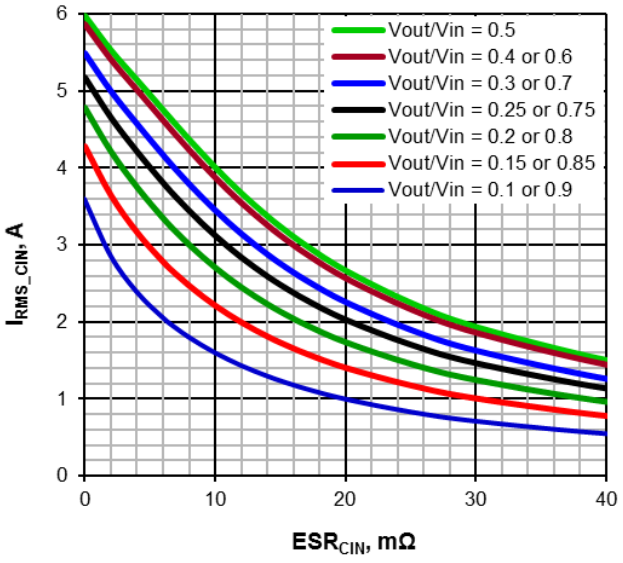
For V_{OUT} ≤ 2 V, the maximum allowed capacitance is 5000 µF. In the example, 7x 330 µF/50 mΩ capacitors are needed. This is a total capacitance of 2310 µF, which is well below the maximum allowed. When V_{OUT} ≥ 2 V, the maximum capacitance is 10000 µF / V_{OUT}. For example, with V_{OUT} = 3.3 V, the maximum allowed capacitance is 3030 µF.

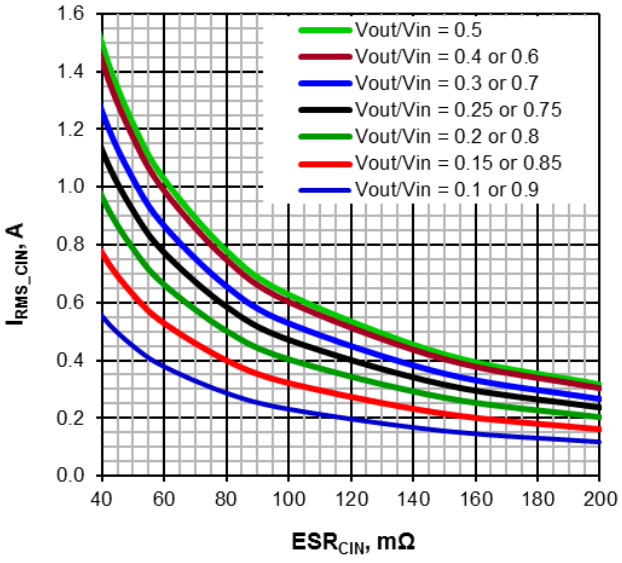
The output voltage ripple can be evaluated through simulation using the circuit below. This circuit incorporates worst-case conditions that include the effects of component tolerances, temperature extremes (-55 °C to 125 °C), radiation (100 krad), and aging (10 year mission). Note that the resistor shown in series with the inductor includes the resistance of the inductor and ISL70002 power FETs. The pulsed voltage source should have a peak voltage equal to the input voltage and the minimum switching frequency (425 kHz) to evaluate the worst-case ripple. The duty cycle should be adjusted to attain the correct output voltage.



6.2.6 Input Capacitors

A minimum input capacitance of 100 µF should be added between VIN and GND to maintain the input voltage during transient conditions. The SVPL3R312SG has been designed with internal ceramic input capacitors to minimize the voltage stresses on its power MOSFETs. These ceramic capacitors also reduce the current stress in the user-added input capacitors. For 100 µF or greater capacitors, the RMS currents of the added capacitors will be determined primarily by their combined ESR. The curves below estimate the total RMS current in the added input capacitors for different V_{OUT}/V_{IN} ratios. Worst-case conditions for load current, internal capacitance, and switching frequency are used. To verify the capacitors will have sufficient margin, the RMS current ratings of the added capacitors can be compared to the appropriate curve. If the application V_{OUT}/V_{IN} ratio is between two curves, use the curve with higher RMS current to be conservative. If multiple capacitors are added, then the RMS current will divide between them. If the maximum application load current is less than the SVPL3R312SG maximum of 12 A, then the RMS current will be reduced proportionally.





For example, let us assume Vin = 5 V, Vout = 1.8 V, max Iout = 9 A, and maximum temperature = 85 °C. Also, assume the capacitor being considered is a 150 µF capacitor with an ESR of 30 mΩ and RMS current rating of 2.7 A at 85 °C. First, determine the Vout/Vin ratio:

$$\frac{V_{out}}{V_{in}} = \frac{1.8V}{5V} = 0.36$$

The ratio lies between the 0.3 and 0.4 curves. Use the Vout/Vin = 0.4 curve, as it has higher RMS current and gives a more conservative estimate. At 30 mΩ, the 0.4 curve indicates an RMS current of 1.85 A. The RMS current for this application is found as:

$$I_{RMS_CIN} = I_{RMS_CURVE}\left(\frac{Application \max I_{out}}{SVPL \max I_{out}}\right) = 1.85A\left(\frac{9A}{12A}\right) = 1.39A$$

The RMS current in the added input capacitors is 1.39 A, which is 51% of the 2.7 A current rating. The power dissipated in the capacitor will be about 26% of its power rating ($0.51^2 = 0.26$).

6.3 PROTECTION FEATURES

6.3.1 Input Undervoltage Lockout

The SVPL3R312SG Series provides input undervoltage lockout (UVLO) protection. For input voltages below the turn-on voltage, the converter will remain off. The internal power MOSFETs will be turned off, and the SVPL3R312SG power stage will be in a high-impedance state. When the input voltage exceeds the turn-on voltage, the converter will start. For input voltages above the UVLO turn-off voltage but below the operating range of the converter, the converter may reach its maximum duty cycle and the output may be out of regulation.

6.3.2 Output Soft-Start

The SVPL3R312SG Series utilizes an output soft-start function to ramp the output in a controlled manner, eliminating output voltage overshoot and limiting inrush current at turn on. A voltage mode soft-start ensures the output waveform remains consistent regardless of changes in the load current. The output rise time is approximately 4 ms. The soft-start function is active whether the module is turned on with an application of input voltage or from driving EN high. The turn-on delay time is specified from the application of input voltage (or application of EN) until the output reaches 90% of its final value.

6.3.3 Output Short Circuit Protection

The SVPL3R312SG Series provides hiccup-mode output short-circuit protection. When a sustained high peak current is detected, the converter will shut down. After a delay, the converter will attempt a soft-start. This sequence will continue until the fault is removed, allowing the converter to soft-start and resume normal operation.

6.4 THERMAL CONSIDERATIONS

The SVPL3R312SG is rated for full power operation at 125 °C. Above 125 °C, the output power must be derated linearly from full power at 125 °C to zero power at 135 °C. The operating temperature of the converter is specified on the baseplate of the converter. The converter is designed to be conduction-cooled, with the baseplate mounted to a heat sink, chassis, PCB, or other thermal surface. The internal power-dissipating components are mounted to the baseplate of the converter and all heat flow is through the baseplate. The lid of the converter does not provide a good thermal path.

The maximum temperature rise from junction to case is 18 °C at full load.

6.5 VPT RHA PLAN AND APPROACH

VPT takes a conservative approach to radiation testing to ensure product performance during space travel. VPT's DLA approved Radiation Hardness Assurance (RHA) plan documents VPT's processes and procedures for guaranteeing the performance of VPT products under various environmental conditions in space, including TID, SEE, and ELDRS.

Documents Available	Details
DLA approved Radiation Hardness Assurance (RHA) Plan Summary	The radiation environments covered by this overview include: total ionizing dose (TID), which includes enhanced low dose rate sensitivity (ELDRS); displacement damage (DD); and single event effects (SEE).
Worst-Case Analysis Report	Detailed worst-case analysis guarantees circuit performance post radiation and end of life.
Stress Report	Individual component stress analysis and deratings are included as part of the WCA report.
Radiation Test Summary Report	An overview report on the component level RLAT and characterization testing for TID and DD as well as the hybrid level characterizations for TID and SEE response.
Reliability Report	MTBF report based on MIL-HDBK-217 reliability calculations.
Thermal Analysis Report	Component temperature rise analysis and measurement results.

Test Definition	VPT's Approach
Total Ionizing Dose (TID). A measure of the energy absorbed in the semiconductor components from the naturally occurring sources of radiation (protons, electrons, photons). This results in the slow degradation of semiconductor performance specifications. TID is tested by exposing components to gamma radiation from a Cobalt-60 source.	Designed for 100 krad(Si). Sensitive semiconductor components undergo RLAT to 100 krad(Si) per MIL-STD-883 Method 1019. Converters are characterized to 100 krad(Si).
Enhanced Low Dose Rate Sensitivity (ELDRS): Many linear-bipolar integrated circuits show enhanced parameter degradation when exposed at low dose rates close to those seen in a space environment as compared to the high dose rates (50-300 rad(Si)/s) that components were traditionally tested at for TID degradation. MIL-STD-883 Method 1019 gives guidance for characterizing components for ELDRS. Components that exhibit ELDRS are tested for TID at a rate below 0.01 rad(Si)/s.	All bipolar linear ICs are verified to be ELDRS free in accordance with MIL-STD-883 test method 1019 section 3.13
Single Event Effects (SEE). Single high energy protons and heavy ions can deposit sufficient energy in a semiconductor component, causing a range of effects. SEEs include single event latchups (SELs), single event gate ruptures (SEGRs), single event transients (SETs), single event functional interrupts (SEFIs) and single event burnouts (SEBs).	Converters are characterized for catastrophic events (SEL, SEB, SEGR) as well as functional interrupts (SEFI) under heavy ion exposure to LET = 85 MeV-cm^2/mg. Converters are also characterized for cross section and magnitude of output transients (SET) for at least 3 different LET levels.
Displacement Damage (DD) is caused by protons and neutrons. Particles displace atoms in the bulk silicon crystal structure. DD leads to a darkening of optics and gradual degradation of performance. DD is tested at the component level with a neutron source.	Optoisolators are not used. The sensitive semiconductor component is characterized by the manufacturer for DD performance to 1x10^{12} n/cm^2.
Radiation Lot Acceptance Testing (RLAT): Semiconductor wafer lots are exposed to TID or neutron radiation on a sample basis. If the parameter degradation for the tested samples is within the predetermined acceptance limits, then the lot can be used in radiation hardened converters.	Sensitive semiconductor component undergoes RLAT for TID.

7.0 ENVIRONMENTAL SCREENING

100% tested per MIL-STD-883 as referenced to MIL-PRF-38534.

Contact sales for more information concerning additional environmental screening and testing options. VPT Inc. reserves the right to ship higher screened or SMD products to meet orders for lower screening levels at our sole discretion unless specifically forbidden by customer contract.

Test	MIL-STD-883 Test Method, Condition	/H+ (Class H + PIND)	/K (Class K)	/EM (Engineering Model) Non-QML[1,6]
Non-Destructive Bond Pull	TM2023	•[2]	•	•[2]
Internal Visual	TM2010, TM2017, TM2032 (MIL-STD-750, TM2072, TM2073)	•	•	•
Temperature Cycling	TM1010, Condition C -65 °C to 150 °C, Ambient	•	•	
Constant Acceleration	TM2001, 3000g, Y1 Direction	•	•	
PIND[3]	TM2020, Condition A	•[2]	•	
Pre Burn-In Electrical	25 °C		•	
Burn-In	TM1015, 320 hrs., 125 °C, Case Typ		•	
	TM1015, 160 hrs., 125 °C, Case Typ	•		
	24 hrs., 125 °C, Case Typ			•
Final Electrical	MIL-PRF-38534, Group A Subgroups 1-6 -55 °C, 25 °C, 125 °C[4]	•	•	
	MIL-PRF-38534, Group A Subgroups 1 and 4 25 °C			•
Hermeticity (Seal)	TM1014, Fine Leak, Condition A2 or B1	•	•	
	TM1014, Gross Leak, Condition C1 or B2	•	•	
	Gross Leak, Dip ($1x10^{-3}$)			•
Radiography[5]	TM2012		•	
External Visual	TM2009	•	•	•

1. Non-QML products may not meet all requirements of MIL-PRF-38534
2. Not required per MIL-PRF-38534. Test performed for additional product quality assurance
3. PIND test Certificate of Compliance included in product shipment
4. 100% R&R testing with all test data included in product shipment
5. Radiographic test Certificate of Compliance and film(s) or data CD included in product shipment
6. Engineering models utilize only the screening specified and are not considered compliant for flight use

8.0 STANDARD MICROCIRCUIT DRAWING (SMD) NUMBERS

Standard Microcircuit Drawing Number	SVPL3R312SG Series Similar Part Number
5962R1721701HYC	SVPL3R312SGN/H+
5962R1721701HXA	SVPL3R312SG/H+-E
5962R1721701KYC	SVPL3R312SGN/K
5962R1721701KXA	SVPL3R312SG/K-E

Do not use the SVPL3R312SG Series similar part number for SMD product acquisition. It is listed for reference only. For exact specifications of the SMD product, refer to the SMD drawing. SMDs can be downloaded from the DLA Land and Maritime (Previously known as DSCC) website at https://landandmaritimeapps.dla.mil/programs/defaultapps.asp. The SMD numbers listed above represents the Federal Stock Class, Device Type, Device Class Designator, Case Outline, Lead Finish and RHA Designator (where applicable). Please reference the SMD for other screening levels, lead finishes, and radiation levels. All SMD products are marked with a “Q” on the cover as specified by the QML certification mark requirement of MIL-PRF-38534.

9.0 ORDERING INFORMATION

SVPL	3R3	12	S	G		/K	-	E
1	2	3	4	5	6	7		8

(1) Product Series	(2) Nominal Input Voltage	(3) Output Current	(4) Number of Outputs	(5) Package Option	(6) Package Lead Option[4]	(7) Screening Code[1,2,3]	(8) Additional Screening Code[4]
SVPL	**3R3** 3.3 Volts	**12** 12 Amps	**S** Single	**G** Gullwing	**None** Formed **N** Straight	**/EM** Engineering Model **/H+** Class H + PIND **/K** Class K	**E** Solder Dipped Contact Sales for additional options

1 Contact the VPT Sales Department for availability of Class H (/H) or Class K (/K) qualified products
2 VPT Inc. reserves the right to ship higher screened or SMD products to meet lower screened orders at our sole discretion unless specifically forbidden by customer contract
3 Engineering models utilize only the standard screening specified and are not considered compliant for flight use. These models are intended for low volume engineering characterization only and have no guarantee regarding operation in a radiation environment. The customer must place the following statement on each line item of their purchase order(s) for /EM units when ordering engineering models:

“(Customer Name) acknowledges that the /EM unit listed in this line item is not permitted for flight use and will be used for Engineering characterization only.”

4 When selecting Package Lead Option “Formed”, Additional Screening Code “-E” (solder dipped leads) must also be applied. When selecting Package Lead Option “Straight”, Additional Screening Code “-E” should not be applied.

Please contact your sales representative or the VPT Inc. Sales Department for more information concerning additional environmental screening and testing, different input voltage, output voltage, power requirements, source inspection, and/or special element evaluation for space or other higher quality applications.

10.0 CONTACT INFORMATION

To request a quotation or place orders please contact your sales representative or the VPT, Inc. Sales Department at:

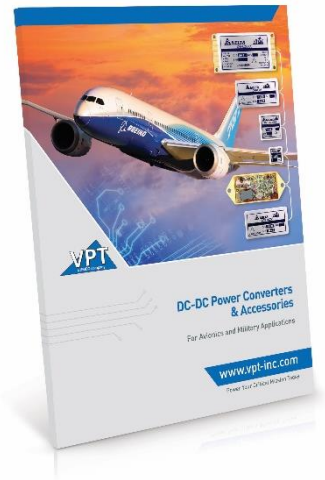
Phone: (425) 353-3010
Fax: (425) 353-4030
E-mail: vptsales@vptpower.com

All information contained in this datasheet is believed to be accurate, however, no responsibility is assumed for possible errors or omissions. The products or specifications contained herein are subject to change without notice.

11.0 ADDITIONAL INFORMATION

Visit the VPT website for additional technical resources, including:

Product Catalogs



Application Notes and White Papers



Technical Video Labs



Additional Products For Avionics/Military, Hi-Rel COTS, and Space Applications

